Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1, 14, 19 and 29-32 have been amended. No claims have been cancelled. Therefore, claims 1-32 are presented for examination.

Claim 30 stands objected to because there are two claims numbered as "30". The claims have been amended to overcome this objection. Applicant submits that the claims have been renumbered as suggested by the Office Action

Claims 1, 2, 4, 14, 19, and 30 stand rejected under 35 U.S.C. §102(b) as being anticipated by Min (U.S. Patent No. 6,184,907). Applicants submit that the present claims are patentable over Min.

Min discloses a computer graphics subsystem (or graphics accelerator) for performing graphic data processing in a computer system. The graphics accelerator is connected to a host processor (CPU) via a host bus. The graphics accelerator is further connected to a frame buffer that stores R (red), G (green), B (blue) video data, as well as additional colors and/or grey scale data, generated by application programs which are executed in host processor 200. The graphics accelerator is further connected with a computer display device and/or a television display. In the graphics accelerator, a host interface is connected to the host bus and provides interface associated with host processor. A graphics engine manipulates the video data stored in the frame buffer in accordance with commands and data from host processor 200. A display controller 130 generates horizontal and vertical synchronizing signals H-SYNC and V-SYNC which are applied to control the display device. The controller 130 further generates a display enable signal D_EN synchronized with the horizontal synchronizing signal H-SYNC, which designates display enable periods. A FIFO

buffer 140 includes FIFO storage space for buffering the video data provided by frame buffer. The FIFO buffer includes a RAM array for data storage, and generates a memory read request signal M_RQ when there are any vacant storage locations available in the RAM array. A memory controller controls the read operation of frame buffer at the request of FIFO buffer, i.e., in response to the memory read request signal M RQ, and further controls the write operation of FIFO buffer via signal W_EN. See Min at col. 3, ll. 58 – col. 4, ll. 55.

The RAM array within the FIFO buffer includes first and second storage regions A and B of identical storage capacity, and stores video data provided by the frame buffer. The buffer further includes control logic, a write pointer, two read pointers and an address selector 360. The control logic generates a plurality of control signals associated with video data buffering, as well as memory read request signal M RQ. Specifically, the control logic generates a write strobe signal W_ST in response to a write enable signal W_EN provided from the memory controller (col. 5, ll. 16-30).

Claim 1 of the present application recites a queue mechanism divided to include a first functional unit block (FUB) to perform a first set of functions for the queue mechanism and a second FUB to perform a second set of functions for the queue mechanism. Applicants submit that Min does not disclose such a queue mechanism. Instead, Min discloses a FIFO buffer having first and second storage regions with identical storage capacity. Nonetheless, the storage regions are not divided to perform separate sets of queue functions. As a result, claim 1 is patentable over Min.

Claims 2-13 depend from claim 1 and include additional features. Thus, claims 2-13 are also patentable over Min.

Claim 14 recites a queue mechanism divided to include a first functional unit block (FUB) to perform a first set of functions for the queue mechanism and a second FUB to perform a second set of functions for the queue mechanism. Therefore, for the reasons described above with respect to claim 1, claim 14 is also patentable over Min. Since claims 15-18 depend from claim 14 and include additional features, claims 15-18 are also patentable over Min.

Claim 19 recites a queue mechanism comprising a first functional unit block (FUB) to perform a first set of functions for the queue mechanism and a second FUB to perform a second set of functions for the queue mechanism. Accordingly, for the reasons described above with respect to claim 1, claim 19 is also patentable over Min. Because claims 20-29 depend from claim 19 and include additional features, claims 20-29 are also patentable over Min.

Claim 30 recites a queue mechanism divided to include a first functional unit block (FUB) to perform a first set of functions for the queue mechanism and a second FUB to perform a second set of functions for the queue mechanism. Thus, for the reasons described above with respect to claim 1, claim 30 is also patentable over Min. Since claims 31 and 32 depend from claim 30 and include additional features, claims 30 and 32 are also patentable over Min.

Claims 3, 5-13, 15-18, 20-29, and 31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Min (U.S. Patent No.6,184,907) in view of Cavanna et al. (U.S. Patent No. 6,208,703). Applicants submit that the present claims are patentable over Min even in view of Cavanna.

Cavanna discloses a one stage first-in-first-out synchronizer that includes a producer side and a consumer side. The producer side includes a first write buffer, a not full output, a write input, a second write buffer and a write clock input. The first write buffer stores a write pointer. The not full output indicates whether new data may be written. The write input is asserted to write data. The second write buffer receives as input a read pointer. The write clock input is used to provide a clock signal to the first write buffer and the second write buffer. The consumer side includes a first read buffer, a not empty output, a read input, a second read buffer, and a read clock input. The first read buffer stores the read pointer. The not empty output indicates whether stored data may be read. The read input is asserted to read data. The second read buffer receives as input the write pointer. The read clock input is used to provide a clock signal to the first write buffer and the second write buffer. See Cavanna at Abstract.

Nonetheless, Cavanna does not disclose or suggest a queue mechanism comprising a first functional unit block (FUB) to perform a first set of functions for the queue mechanism and a second FUB to perform a second set of functions for the queue mechanism. As discussed above, Min does not disclose or suggest such a feature. Thus, any combination of Min and Cavanna would also not disclose or suggest the feature. Consequently, the present claims are patentable over Min in view of Cavanna.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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